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A Review Paper on A 10 Bit, Low Power ADC Suitable for Wireless Application

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Abstract: This Paper presents the Design of analog to digital converter(ADC) for wireless applications, so here is the selection of right architecture is very crucial. We have chosen successive approximation Analog to Digital Converter because of their compact circuitry as compared with the Flash ADC which makes this SAR ADC inexpensive. Day By Day more and more applications are built on the basis of power consumption so this SAR ADC will be useful for high speed with medium resolution and low power consumption. The Successive Approximation (SAR) architecture is very suitable for data acquisition, it has resolutions ranging from 8 bits to 12 bits and sampling rates ranging from 50 KHz to 50 MHz.

Keywords: Successive Approximation Register (SAR),Low power, Resolution, Sampling Rate.

I. INTRODUCTION

In many mixed-signal systems, Analog-to-Digital Converters (ADC) are required for interfacing analog signals to digital circuits[8]. Sigma Delta ADC architectures are very useful for lower sampling rate and higher resolution (approximately 12-24 bits). The common applications for Sigma-delta ADC architecture are found in voice band, audio and industrial measurements. The Successive Approximation (SAR) architecture is very suitable for data acquisition, it has resolutions ranging from 8 bits to 12 bits and sampling rates ranging from 50 KHz to 50 MHz. The most effective way to create a Giga rate application with 8 to 16 bit resolution is the pipeline ADC architecture. Here in this we are presenting SAR ADC because in the past few years, more and more applications are built with very stringent requirements on power consumption. For electronic systems, such as wireless systems or irnplantable devices, the power consumption is becoming one of the most critical factors. SAR ADC is known for its simple structure, thus consuming less power and saving more die size[1].This SAR ADC also use in Ultra Wide Band(UWB) radio technology. UWB receivers require high-speed but low-resolution analog-to-digital converters (ADCs), in the range of 4–5 bits. Pipelined ADCs are used for high-speed, medium-resolution applications. They can provide one conversion per clock period throughput and only a linear scaling in complexity with resolution; however, they rely on operational amplifiers at the heart of the multiplying digital-to-analog converter (MDAC) in each pipelined stage. Because it must be closed loop stable, this amplifier typically uses one or two high gain stages. Unfortunately, in deep-submicron CMOS, the achievable gain per stage is limited because short-channel effects lower $g_m r_0$ for a single transistor, and reduced voltage supplies restrict circuit techniques such as cascoding. Thus, there are significant challenges for continued scaling of pipelined ADCs[2]. Thus. this SAR ADCs are commonly used in biomedical acquisition systems due to their low power consumption and simplicity, particularly for simple analog sub-circuits. This SAR ADC consist of sample and hold circuit, a comparator, Successive approximation register and control logic and DAC.

II. RELATED WORK

An increasing number of IC compatible sensors demand suitable readout circuits with on-chip ADC to reduce the signal sensitivity to perturbations on the circuit and at the sensor interface, decrease system complexity and cost, as well as enable further on-chip digital processing like data correction. Applications like wireless sensor nodes and medical diagnose always require at least 12-bit linearity and noise performance and extremely low power consumption (as low as 100μW) because of the battery operation . In addition, to meet the requirements of large sensor arrays, the ADC must occupy small silicon area and can be multiplexed between multiple channels.. A 100μW, 13bit ADC used for sensor array applications is presented in paper [1].

The ADC employs an extended counting architecture in which the residual error from a first-order incremental ΣΔ modulator is encoded by a cyclic ADC to achieve high accuracy at a relatively high speed. Hardware reuse technique is utilized for low power consumption and small silicon area. The prototype ADC is implemented in 0.18μm CMOS technology with 1.8V supply voltage and the core area is only 0.06mm2 including control logic. The ADC shows a peak SNDR/SFDR of 65.4dB/71.9dB.

RFID is one of the modern applications of RF technology. In general, RFID is an Identification system like other techniques such as classic barcodes and biometrics. Usage of RFID is growing intensively in these days, as you can see it in supermarkets for cashless payment, warehousing, asset management and also airport baggage control, library management, medical monitoring and access/security control. So in this paper[2], SAR ADCs have been mostly used for moderatespeed,

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moderate-resolution pplications that power consumption is one of the major concerns (e. g. RFID). Furthermore two-step ADCs are classified as high-speed, low to moderate-accuracy ADC. In this paper an ultra low power two-step-SAR ADC for RFID application is presented. Several techniques are used to further reduce the power consumption and relatively elevate the speed of the ADC. These techniques include a low power comparator with no static current and a dual-stage (Resistorstring / capacitive dividing) architecture as digital-to-analog converter (DAC). In this DAC architecture fine search will be performed by only two C and 15C capacitors which reduced the silicon area significantly. The circuit designed in 0.18um CMOS technology and simulations show that the 8-bit ADC, consumes almost 166nW at 11.25kS/s. The results show that the proposed ADC has higher speed with almost the same power consumption in comparison with its charge redistribution counterpart.

Analog to Digital Converter is one of the most critical parts in transceiver design. The common design parameters of an ADC are conversion rate and resolution. To be used in WiMAX system with 10MHz maximum input signal, pipeline architecture has been chosen. The 12-bit, 40MS/s ADC presented in this work, built in eleven stage sub ADC without digital error correction. In this paper[3], 12-bit, 40 MS/s Pipeline Analog to Digital Converter is designed for application in WiMAX system. Eleven stages pipeline architecture, consist of ten stages 1.5-bit sub ADC and one stage 2-bit flash ADC. The Project was built until simulation level in SIMetrix software, using AMS BiCMOS 0.35um SiGe transistor's model. The simulation showed the ADC has 28dB SFDR.

For dynamic testing of ADC, standard histogram technique with sine wave input is most popular in addition to the Fast Fourier Transform (FFT) and sine wave curve fitting technique. If the input to an ADC is other than sine wave or triangular wave then parameters determined with these inputs are not useful. Usually manufacturer of a device provides specification in its data sheet under certain test conditions. If application conditions of a user of a device are other than user conditions then data sheet specifications will not be very
much useful for user's application. If the aim is to select a better device for an application then data sheet specifications are sufficient for comparison. But if a selected device is to be used in a design then determination of its functional parameters over application condition is must. In this work we are developing method for dynamic testing of an ADC using application input. This testing will be useful rommanufacturer's point of view as well as user's point of view. Due to high cost of ADC and its test instruments development of dynamic test methods are carried out by simulation through software. Test methods developed by simulation are equally suitable for testing a real life ADC in application condition with minor changes related with hardware and software. Standard histogram technique is based on determination of DNL by probability estimation and also code transition levels are determined by cumulative histogram based upon phase estimation. As far as multi-frequency application signals are concerned, it is extremely difficult to derive a formula for DNL based upon probability estimation and also code transition level based upon phase estimation. Similarly determination of ENOB of an ADC using sine wave curve fitting technique is extremely difficult, if not impossible for application input. For FFT technique using multiple frequency application signal, reproduction of baseband spectrum at regular interval at sampling rate makes it very difficult to accurately determine frequency, amplitude and phases of different components of the input. Hence, for testing an ADC for an arbitrary input either totally different approach or suitable modifications are needed in existing test methods. In our proposed approach we are determining different sinusoidal components of application input by applying IFFT algorithm. For this purpose, very high resolution and highly accurate spectrum analyzer can be used for determining components of application input. Further these determined components of application input are used to
simulate application input through software and their samples are collected by digitizing through a simulated ADC.so this paper[4] presents a new approach for determination of nonlinearity and Effective Number of Bits (ENOB) of an Analog to Digital Converter (ADC) for application input. Many times the input to ADC in an application is other than standard signals such as sine wave or triangular wave. Parameters of ADC determined using dynamic testing with standard signals are not useful if input signals are different. Different sinusoidal components of application input can be determined by spectrum analyzer. Application input can be generated by downloading data points created by computer in an Arbitrary Waveform Generator (AWG). Differential Nonlinearity (DNL) of an ADC is determined using deviation of actual histogram from reference or ideal histogram. Further estimation of Integral Nonlinearity (INL) is done from summation of DNL. ENOB is determined by estimating ideal rms error and actual rms error. These rms errors are computed by taking difference of sampled ADC input value available in computer and corresponding ADC output. Simulation results for 5 and 8 bit ADCs are reported and experimental results for an actual 8 bit ADC are also reported.. Comparison of simulation results by proposed method is done for standard sine wave, triangular wave and application inputs. It is expected that this work will initiate research toward ADC testing using application input.

The recent advancement in bioelectronics and its applications in implantable human-IC interface have urged for the development of advanced circuit techniques with microwatt level power consumption. In such systems, every single nW of power is valuable. Therefore each individual block must be carefully scrutinized. Their analog front end usually consists of several building blocks such as pre-amplifier, bandpass filter, analog-to-digital converter (ADC) and Mux, etc , among which the ADC is a major power consumption contributor. Hence, designing a low-power ADC is one of the most important tasks to prolong the life time of the usually battery-powered or battery-less implantable ICs. So in this paper[5] presents a 9-bit 25 kS/s SAR ADC in 0.18 μm CMOS technology for neural signal recording

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applications. The ADC is powered by a single supply voltage of 1V to comply with other digital processing units on the same chip. The proposed ADC has one common-mode DC input of 0.5V thus offering a full-range sampling with only one pair of PMOS input transistors in the latched comparator. A versatile digital interface block is implemented to translate external control signals to internally useful Sample-and-Hold (S/H) commands, allowing a flexible S/H duration to match with the driving strength of the input buffer. To realize an ultra low-power performance, all digital blocks and the comparator are carefully optimized. At the same time, split-cap architecture with an attenuation cap is used to minimize area and to further reduce the power consumption. Our simulation shows that the proposed SAR archives 8.5 ENOB while consuming only 160 nW.

In the last few years, there has been a growing interest in the design of wireless sensing device for portable, wearable or implantable biomedical applications. These sensing devices are generally used for detecting and monitoring biomedical signals such as electrocardiographic (ECG), electroencephalography (EEG), and electromyography (EMG), to name a few. Most biomedical signals are often very slow and exhibit limited dynamic range. A typical biomedical sensor interface consists of a band-pass filter, a low-noise amplifier and an analog-to-digital converter (ADC). The digitalization of the sensed biomedical signals is usually performed by ADCs with moderate resolution (8–12 bits) and sampling rate (1–1000 kS/s) . In such devices, energy efficiency and long battery life are paramount design goals. Particularly, ADCs for implanted medical devices need microwatt operation to run on a small battery for decades . Therefore, energy efficiency is a critical challenge for ADCs design. This paper[6] presents an energy efficient successive-approximation- register (SAR) analog-to-digital converter (ADC) for biomedical applications. To reduce energy consumption, a bypass window technique is used to select switching sequences to skip several conversion steps when the signal is within a predefined small window. The power consumptions of the capacitive digital-to-analog converter (DAC), latch comparator, and digital control circuit of the proposed ADC are lower than those of a conventional SAR ADC. The proposed bypass window tolerates the DAC settling error and comparator voltage offset in the first four phases and suppresses the peak DNL and INL values. A proof-of-concept prototype was fabricated in 0.18-µm 1P6M
CMOS technology. At a 0.6-V supply voltage and a 200-kS/s sampling rate, the ADC achieves a signal-to-noise and distortion ratio of 57.97 dB and consumes 1.04 µW, resulting in a figure of merit of 8.03 fJ/conversion-step. The ADC core occupies an active area of only 0.082 mm .

III. PROPOSED WORK

Up till now the design of the Successive Approximation Analog to Digital Converter has been implemented with good resolution in particular higher nanometer technology having good sampling rate. So if we implement this SAR ADC with higher sampling rate then the technology will be increased. So we will implement this SAR ADC having Resolution of 8 bit with sampling rate in Mega Samples Per Second in reduction in its nanometer technology. So for designing such Compact Low Power SAR ADC, it provides less chip size also minimization of power takes place. This Proposed SAR ADC will be designed in Tanner Tool V15.0 /ADS Tool. Performance evaluation will based on the implementation results obtained through this tool.

Generalised Block Diagram of SAR ADC:

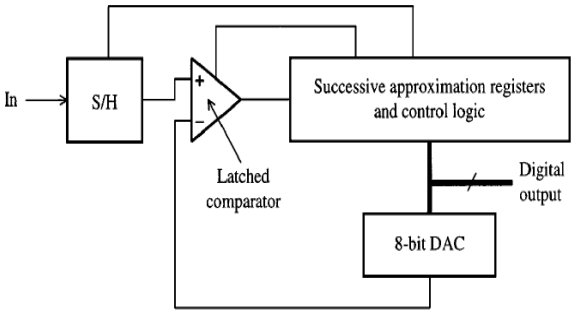

Fig : General Block Diagram of SAR ADC

Advantages:

The main advantage of SAR ADC is good ratio of speed to power. The SAR ADC has compact design compare to flash ADC, which makes SAR ADC inexpensive. This SAR ADC will be useful for high speed with medium resolution and low power consumption.

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